22. (Amended) An information processing system according to claim 18, wherein said memory stores therein instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code from the memory and along the first memory bus to said buffer and said control circuit prefetches the operand data from the memory and along the second memory bus to said buffer.

29. (Amended) An information processing system according to claim 18, wherein said access judging circuit prefetches instruction code from said memory along said first memory bus and into the buffer.